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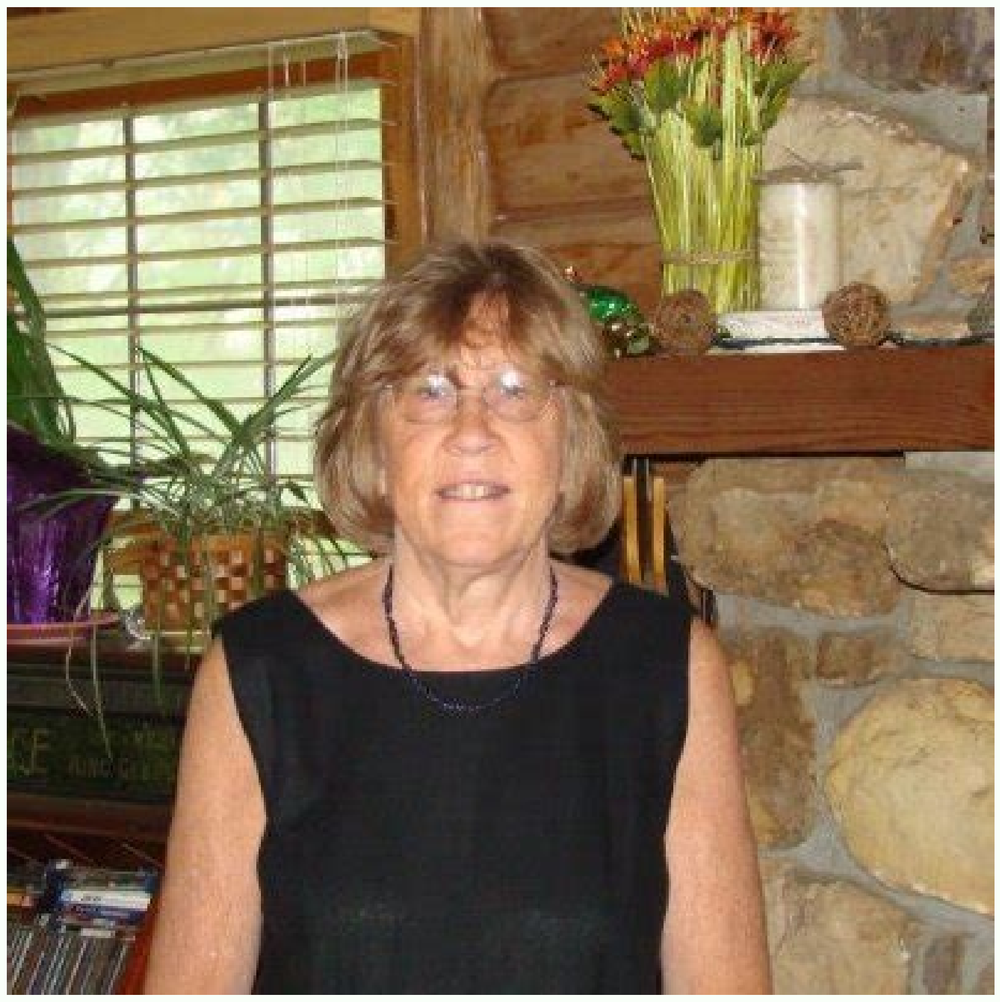

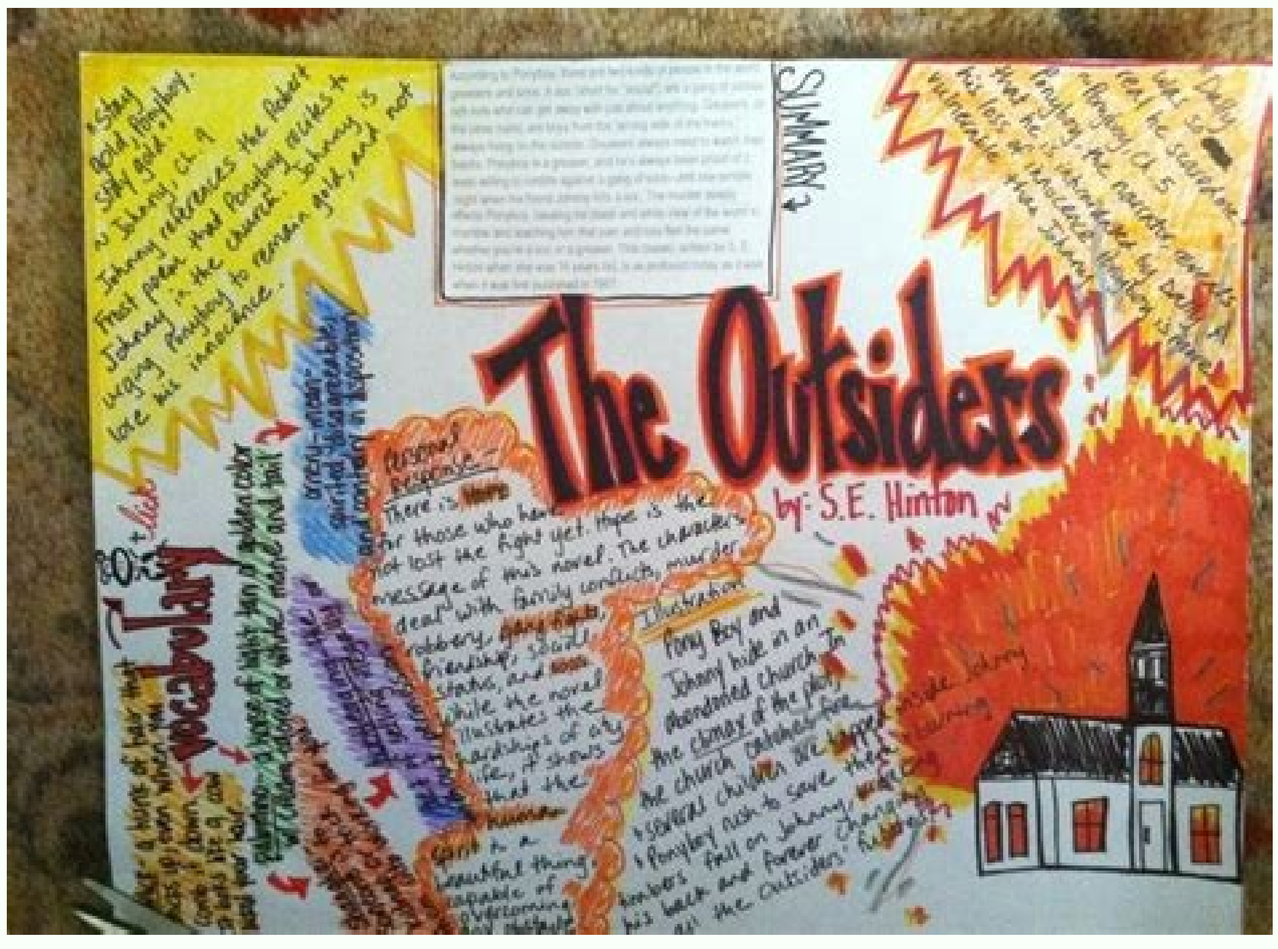

Experience (years)	Grade (form)
6	1
12	2
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, a free encyclopedia that anyone can edit. 6,579,370 articles in English "Restoration of Life" in which Phosphatodraco is depicted in an earthly pose. Phosphatodraco is a genus of azhdarchid pterosaurs that lived in the Late Cretaceous in what is now Morocco. In 2000, a pterosaur specimen consisting of five cervical vertebrae was found in the Ouled Abdun phosphate pool. The specimen was made the holotype of the new genus and species Phosphatodraco mauritanicus in 2003. It is one of the last known pterosaurs, and its neck is one of the best-preserved of the azhdarchids. Due to the fragmentation of the vertebrae of the holotype, it is unclear how Phosphatodraco differs from other azhdarchids and how large it is: its wingspan may have been 4 m (13 ft) or 5 m (16 ft). Its neck may have been 865 mm (2 ft 10 in) long. It would have had a proportionally long neck, small body, and long limbs compared to other pterosaurs. The diversity of pterosaur taxa in the Ouled Abdun Basin, including Phosphatodraco, just before the Cretaceous–Paleogene extinction event suggests that the pterosaur extinction occurred suddenly. (Full article...) Recently added: Katherine D. Sullivan Niandra Ladès and usually just a Betsy Bakker-North t-shirt Email archive Other selected articles on the Eatoniella mortoni holotype... that the New Zealand mussel Eatoniella mortoni (pictured) may evolve into an environment rich in exceptionally high levels of carbon dioxide, making it the focus of ocean acidification research? ...that a global coalition to save Abu Simbel, Philae and many other temples led to today's World Heritage List? ... that spatial inequality refers to the unequal distribution of income and resources between geographic regions? ...that an interdisciplinary study showed that Motilla del Azuer was built while irrigating 4.2 km BP during a long period of severe drought? ... that Grumman Aerospace has built its own power plantwas it cheaper than buying electricity from the grid? ... that the researchers misnamed 1T-SRAM MoSys "with a catchy name"? ...that in protest of Rowe's dismissal of Wade's case, Billie Eilish played a song that criticizes violent people in power? ... that Maria Urquidez was the "mother of bilingual education"? Archive Start a new article Assign an article Hénoc Muamba An earthquake near the city of Chianjur in West Java, Indonesia, has killed at least 271 people and injured more than 2,000. In Canadian football, the Toronto Argonauts defeat the Winnipeg Blue Bombers in the Gray Cup (pictured is MVP Henok Muamba). The International System of Units officially recognizes the metric prefixes quetta-, ronna-, ronto-, and quecto-. NASA Artemis 1 successfully launched an unmanned test flight to the Moon. Ongoing: World Cup Mahsa Amini Protests Russian Invasion of Ukraine Recent Deaths: Cecilia Sweet Marshall John E. Brown Jr. Mickey Kuhn Michael Perchuk Jeremy Lloyds Dwight Garner Assign Article November 24: Thanksgiving Day in the United States (2022) D. B. Cooper's 1859 composite drawing FBI - On the Origin of Species by British naturalist Charles Darwin was first published and the first print was sold out on the first day . 1941 – Holocaust: The Terezin Ghetto was established as a stop at the Nazi death camps and a "guesthouse" for elderly and prominent Jews to mislead the public about the Final Solution. 1971 - After collecting a $200,000 ransom, D. B. Cooper parachuted out the back door of a hijacked plane over the Pacific Northwest and disappeared. 2015 A Russian Su-24 attack aircraft was shot down by a Turkish fighter after the fighter reportedly entered Turkish airspace and ignored warnings to change course. Zachary Taylor (1784) Arundhati Roy (1961) Goo Hara (2019) Next Anniversary: November 23 November 24 November 25List of days of the year via email The turkey is a large bird of the genus Meleagris native to North America. There are two extant turkey species: the wild turkey (M. gallopavo) from east-central North America and the ocellata turkey (M. ocellata) from the Yucatan Peninsula of Mexico. This photo, taken at Deer Island Preserve in Novato, California, shows a winged male Rio Grande wild turkey (M.g.intermedia), a courtship display in which the snook (erectile, fleshy bump on the forehead) becomes swollen with blood and turns red . , and lengthens as it hangs well below the beak. Photo Credit: Frank Schulenburg Recently Featured: Cephalanthus occidentalis St Anne's Archives Laetiporus sulphureus Other featured photos Community Site • Editors' Central Hub for resources, links, tasks, and announcements. Country Pump - A forum for discussion of Wikipedia itself, including political and technical issues. Website News News sources about Wikipedia and the wider Wikimedia movement. The Tea Room - Ask basic questions about using or editing Wikipedia. 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Asturianu à¦¬à¦¾à¦¦à¦¾ Bosanski Eesti ÍÎ»Î»Î Î½Î¹ÎºÎ¬¬ Plain English Galego Hrvatski LatvieÅ¡u LietuviÅ³ à´®à´²ÐÐþóà´Ðþþà´ ¸ Norsk nynorsk Shqip SlovenÐina Sà¸ina Retrieved from " 2Pseudo-Instatic Random Access Memory introduced the technology. This article lists references, related reading, or external links, but its sources remain unclear as it contains no citations. Help improve this article with more accurate citations. (December 2012) (Learn how and when to remove this template) Types of Computer Memory and Data Storage General Storage Cell Memory Coherence Cache Coherence Storage Hierarchy Memory Access Patterns Memory Map Secondary Storage MOS Moving Gate Storage Continuously Available Computers Areal Density (Mass Storage).) Block (data storage) Object storage Direct Attach Storage Network storage Network storage Block-level storage Single-instance storage Data Structured data Unstructured data Big data Metadata Data compression Data corruption Data sanitization Data degradation Data integrity Data security Data verification Data verification and reconciliation Data recovery storage Data clustering Directory resource sharing File sharing File system Clustered file system Distributed file system Distributed file system for cloud distribution and data warehouse distributed database database database database data warehouse data deduplication data structure data duplication replication (processing) refresh memory memory record infoKnowledge Base Computer File Object File File File Deletion File Copy Backup Core Dump Hexadecimal Data Dump Information Communication Transfer Temporary File Copy Protection Volume (Compute) Boot Sector Master Boot Record Boot Record Disk Array Disk Image Disk Mirroring Disk Summary Storage Partitioning Segmentation Reference Disk Space Logical Disk Storage Virtualization Virtual Storage Memory File Software Entropic Software Red Memory Storage Processing Resilience (Computer Science) Persistent Data Structure RAID No RAID Disk Architecture Storage Bank Paging Grid Switching

Computing Cloud Computing Cloud Storage Fog Computing Edge Computing Dew Computing Amdahl's Law Wall Law Crider's Law Volatile RAM Hardware Cache CPU Cache Notebook Memory DRAM eDRAM SDRAM SGRAM LPDDR QDRSRAM EDO DRAM XDR DRAM RDRAM SDRAM DDR GDDR GRAM Dual Memory Port RAM Vi deo-RAM (Dual-Ported DRA M) Historical Tube Williams-Kilburn (1946-1947) Delay Line Memory (1947) Mellon Optical Memory (1951) Selectron Tube (1952) Dekatron T-RAM (2009) Z-RAM (2002 - 2010) Nonvolatile ROM MROM PROM EPROM EEPROM ROM Cartridge Solid State Storage (SSS) Flash memory is used in: Solid State Drive (SSD) Solid State Hybrid Drive (SSHD) USB Flash Drive IBM FlashSystem Flash Core Module Memory Stick CompactFlash PC Card MultiMediaCard SD Card SIM Card SmartMedia Universal Flash Storage SxS MicroP2 XQD Card Programmable Metallization Cell NVRAM Memistor Memristor PCM (3D XPoint) MRAM Electrochemical RAM (ECRAM) Nano-RAM CBRAM Early NVRAM FeRAM Memory Memory FeRAM Memory Vilindre Memory Electronic Recording Device Magnetic Recording Magnetic Storage Magnetic Tape Magnetic Tape Data Storage Tape Drive Tape Library Digital data storage (DDS) Video tape Videok Asset Cassette Linear open tape Betamax 8mm videoDV MiniDV MicroMV U-matic VHS S-VHS VHS-C D-VHS Hard Drive Optical Optical 3D Data Storage Optical Disc Compact Disc LaserDisc Digital Audio (CDDA) CD Video CD-R CD-RW Video CD Super Video CD Mini CD Optical Discs Nintendo CD-ROM Hyper CD-ROM DVD DVD+R DVD-Video Card DVD DVD-RAM MiniDVD HD DVD Blu-ray Ultra HD Blu-ray Holographic Versatile Disc WORM In Development CBRAM Memory Race Track NRAM Centipede ECRAM Written Multimedia Holographic Data Electronic Holography Quantum optical data storage 5D DNA digital data storage Universal memory time crystal quantum memory UltraRAM historical storage paper (1725) punch (1725) punch (1725) socket delay memory cylinder memory (1932) magnetic core memory (1949) 5 memory, metal (1949)) Main memory (1960s) Thin film memory (1962) Disk array (1962) Twistor memory (~1968) Bubble memory (~1970) Floppy disk (1971) Vte 1T-SRAM is pseudo-static Free access ves memory (PSRAM) technology introduced by MoSys, Inc. in September 1998, which offers a high-density alternative to traditional static random access memory (SRAM) for embedded memory applications. Mosys uses a single-transistor memory cell (bit cell) similar to dynamic random access memory (DRAM), but surrounds the bit cell with control circuitry, making the memory functionally equivalent to SRAM (the controller hides all DRAM-specific operations such as preload and reset). 1T-SRAM (and PSRAM in general) is a standard single-cycle SRAM interface, and the logic surrounding it appears to be the same as SRAM. Using a single transistor bit cell, 1T-SRAM is smaller than conventional (six-transistor or "6T") SRAM and approaches embedded DRAM (eDRAM) in size and density. At the same time, the performance of 1T-SRAM is comparable to multi-megabit SRAM, consumes less power than eDRAM, and is manufactured using a standard CMOS logic process like conventional SRAM. MoSys sells 1T-SRAM as a physical IP address for immediate use.(SOC) applications. It is available for a variety of casting processes including Chartered, SMIC, TSMC and UMC. Some engineers use the terms 1T-SRAM and "embedded DRAM" interchangeably, as some foundries offer MoSys 1T-SRAM as "eDRAM". However, other foundries offer 1T-SRAM as a separate offering. 1T SRAM technology consists of a series of small banks (typically 128 rows × 256 bits/row, for a total of 32 kilobits) connected to a bank-sized SRAM cache and a smart controller. Although space is limited compared to traditional DRAM, the short word lines provide much higher speed, allowing the array to perform a full sense and preload (RAS cycle) on each access, providing high-speed random access. Each access is for one bank, allowing unused banks to be reclaimed at the same time. Likewise, each line read from the active bank is copied into the bank-sized SRAM cache. When repeatedly accessing the same bank that leaves no time for refresh cycles, there are two possibilities: either all are accessed by different rows, in which case all rows are automatically refreshed, or some rows are accessed repeatedly. In the second case, the cache provides the data and allows the unused active bank row to be updated. There are four generations of 1T SRAM: [when?] Original 1T SRAM About half the size of 6T SRAM, less than half the performance. 1T-SRAM-M A variant with lower standby power consumption for applications such as mobile phones. 1T-SRAM-R includes ECC for lower soft error rate. It uses smaller bit cells, which inherently have a higher error rate, to avoid sacrificing area, but ECC more than makes up for it. 1T-SRAM-Q This "quad-density" version uses a slightly non-standard manufacturing process to create a smaller compound capacitor, further halving the memory size compared to 1T-SRAM-R. This slightly increases the manufacturing cost of the wafer, but does not interfere with the fabrication of logic transistors in the conventional DRAM capacitor design.Comparison to Other Embedded Memory Technologies 1T SRAM has comparable speed (at multi-megabit density) to 6T SRAM. That's significantly faster than eDRAM, and the Quad Density option is only slightly higher (claimed 10-15%). At most foundries, eDRAM designs require additional (and expensive) masks and processing steps to offset the cost of the larger 1T SRAM chip. Also, some of these steps require very high temperatures and must be performed after the logic transistors have been formed, which can damage them. 1T-SRAM is also available in component (IC) form. The Nintendo GameCube was the first gaming system to use 1T-SRAM as primary (main) memory. The GameCube has several dedicated 1T SRAM devices. 1T-SRAM is also used in the successor to the GameCube, the Nintendo Wii console. Note that this is not the same as 1T DRAM, which is a "capacitorless" DRAM cell constructed from SOI transistors using a parasitic channel capacitor instead of a discrete capacitor. MoSys claims the following 1T SRAM array sizes: 1T SRAM cell sizes (μm²/bit or mm²/Mbit) Process nodes 250 nm 180 nm 130 nm 90 nm 65 nm 45 nm 6T SRAM bit cell 7.56 4.65 2, 40 1.36 overhead 11.28 7.18 3.73 2.09 1.0.52 1T-SRAM BIT CELL 3.51 1.97 1.10 0.61 0.32 0.15 with overhead 7 .0 1.9 1.1 0.57 0.28 1T-SRAM-Q Bit Cell 0.50 SEL 0.28 0 from Cypress Semiconductor) describes a similar system for hiding a DRAM upgrade using a cache GASH. Literature Glaskowsky, Peter N. (1999-09-13). "MoSys Explains 1T-SRAM Technology: Unique Architecture Hides Updates, Allows DRAM to Work Like SRAM" (PDF). Microprocessor message. 13(12). Retrieved October 6, 2007. Jones, Mark-Eric (October 14, 2003). 1T-SRAM-Q: Quad-Density Technology Limits Growing Memory Requirements (PDF) (Report). MoSys Inc. Retrieved October 6, 2007. The MoSys home page in US Patent No. 6,256,248 shows the DRAM array atthe heart of 1T-SRAM. US Patent No. 6,487,135 uses the term "1T DRAM" to describe the internal structure of 1T SRAM. Youth, Tehfor (16 December 2002). "1T SRAM macros are preconfigured for rapid integration into SoC designs." Archived from the original on July 20, 2019. Retrieved August 21, 2020. Cataldo, Anthony (December 16, 2002). "NEC, Mosys push the frontiers of embedded DRAM". YOUR times. ISSN 0192-1541. Retrieved October 6, 2007. Retrieved from " Computer memory type "DRAM" redirects here. For other uses, see DRAM (disambiguation). This article has a fuzzy citation style. The references used can be made clearer by a different or uniform citation method and footnotes. (April 2019) (Learn how and when to remove this template) Storage and storage types General Storage location Cache coherence Storage coherence Storage hierarchy Storage access patterns Storage mapping Secondary storage Moving gate MOS storage Continuous availability Area density (storage Computer storage) Block (data storage) Object storage Direct Attached Storage Network Storage Block-Level Storage Single Instance Storage Data Structured Data Unstructured Data Big Data Metadata Data Compression Data Corruption Data Sanitization Data Integrity Degradation Data Integrity Data Security Data Validation Verification and Data Reconciliation Data Recovery Storage Data Clustering Directory Sharing File Sharing File System Clustered File System Distributed File System Distributed File System for Cloud Distributed Data Storage Distribution Uj Unified Database Database Data Warehouse Data Warehouse data deduplication Date nstructure Data redundancy Replication (processing) Memory update h Memory storage Information storage Knowledge base Object file Computer file File deletion File copy Backup Memory dump Hex data transfer Data transfer Temporary file Copy protection Digital Rights Management Volume (Computing) Boot sector Master Boot RecordBoot Record Disk Array Disk Image Mirroring Disk Summation Disk Partitioning Storage Segmentation Reference Space Logical Disk Storage Virtualization Storage File Mapped Storage Software Entropy Software Rotation Storage Database Storage Processing Resilience (Computer Science) Non-RAID Data Structure Storage - Paging Bank Switching Network Computing Cloud Computing Cloud Computing Cloud Computing Edge Computing Dew Computing Amdahl's Law Moore's Law Crider's Law Variable RAM Hardware Cache CPU Cache Scratchpad Cache DRAM eDRAM SDDRD XDRSDRAM1 DDRDD SDRAM SGRAM1 -SRAM ReRAM QRAM Addressable memory (CAM) VRAM Dual-port RAM Video RAM (Dual-port DRAM) Historical Williams-Kilburn tube (1946-1947) Delay line memory (1947) Mellon optical memory (1951) La mpa Selectron (1952) Dekatron T-RAM (2009) Z-RAM (2002-2010)) Non-volatile ROM MROM PROM EPRO M EEPROM ROM Cartridge Semiconductor Memory (SSS) Flash S Memory is used in: Solid State Drive (SSD) Hybrid Drive SSD (SSHD) USB Flash Drive IBM FlashSystem Flash Core Module Memory Stick Card CompactFlash PC Card MultiMediaCard SD Card SmartMedia SIM Card Universal Flash Memory SxS MicroP2 XQD Card Programmable Metallization Cell NVRAM Memistor Memristor PCM (3D XPoint) MRAM Electrochemical Random Access Memory (ECRAM) Nano-RAM CBRAM Early Stage NVRAM FeRAM ReRAM FeFET Memory Analog Recording Phonograph Drum Phonograph Recording Quadruplex Video Tape Vision Electronic Recording Equipment Magnetic Recording Magnetic Recording Magnetic Data Storage Tape Drive Tape Library Digital Data Storage (DDS) Video Tape Video Cassette Cassette Tape Linear Tape-Open Video Format Betamax 8mm DV Mini DV MicroMV U-matic VHS S-VHS VHS-C D-VHS Hard Drive Optical 3D Optical Storage Optical Disc LaserDisc Compact Disc Digital Audio (CDDA) CD CD Video CD-R CD-RW Video CD Super Video CD Mini CD Nintendo Optical Hyper CD-ROMsDVD DVD+R DVD-Video DVD Card DVD-RAM MiniDVD HD DVD Blu-ray Ultra HD Blu-ray WORM Holographic Versatile Disc in Development CBRAM Race Track Memory NRAM Centipede ECRAM Memory Recorded Media Holographic Data Storage Electronic Quantum Holography 5D Optical DNA Data Storage Digital data storage Universal Time Crystal Quantum Memory UltraRAM Historical paper data storage (1725) Perforated label (1725) Perforated tape (1725) Plug-in board Linear delay memory Drum memory (1932) Magnetic core memory (1949) Extended wire memory (1957)) Memory Main cable (1960s) Thin film memory (1962) Disk pack (1962) Twistor memory (~1968) Bubble memory (~1970) Floppy disks (1971) vte Micron Technology MT4C1024 DRAM Integrated Circuit Die photo (1994). Its capacity is 1 megabit, which corresponds to 2 20 {\displaystyle 2^{20}} bits or 128 KB.[1] NeXTcube computer motherboard, 1990, with 64 MB main DRAM (top left) and 256 KB video memory [2] (bottom right center). Dynamic Random Access Memory (Dynamic RAM or DRAM) is a semiconductor random access memory that stores each bit of data in a memory cell, usually consisting of a small capacitor and a transistor, both usually based on a metal oxide semiconductor. technology (MOS). While most DRAM cell designs use a capacitor and a transistor, some use only two transistors. In designs that use a capacitor, the capacitor can be charged or discharged; these two states are considered to be two bit values, commonly referred to as 0 and 1. The electric charge of the capacitors is gradually discharged; without intervention, the capacitor data will soon be lost. To prevent this, DRAM requires an external memory recovery circuit that periodically overwrites the data in the capacitors and restores their original charge. This refresh process is a defining characteristic of dynamic random access memory, as opposed to static random access memory (SRAM), which requires no data.Unlike flash memory, DRAM is non-volatile memory (compared to non-volatile memory) because it quickly loses its data when the power is removed. However, DRAM has limited data storage. DRAM is typically an integrated circuit chip that can consist of tens to billions of DRAM memory cells. DRAM chips are widely used in digital electronics where inexpensive, high-capacity computer memory is needed. One of the biggest uses of DRAM is in main memory (colloquially called "RAM") in modern computers and graphics cards (where "main memory" means graphics memory). It is also used in many portable devices and video game consoles. In contrast, SRAM, which is faster and more expensive than DRAM, is typically used where speed is more important than cost and size, such as B. CPU cache. The need to refresh DRAM requires more complex circuitry and timing than SRAM. This is offset by the structural simplicity of DRAM memory cells: only one transistor and one capacitor are needed per bit, compared to four or six transistors in SRAM. This allows DRAM to achieve very high density while reducing cost per bit. Data recovery consumes power and different methods are used to manage the overall power consumption. DRAM price per bit increased by 47% in 2017, the largest jump in 30 years since a 45% jump in 1988, while the price has declined in recent years.[3] As of 2018, "a key feature of the DRAM market is that there are currently only three major vendors, Micron Technology, SK Hynix and Samsung Electronics", which "maintain a relatively small capacity."[4] There is also Kioxia (formerly Toshiba) . Memory Corporation after the split in 2017). exascale supercomputers), individually, e.g.Technology. Others sell them integrated with other products, such as Fujitsu in their processors, AMD GPUs, and Nvidia with HBM2 in some of their GPU chips. History Schematic drawing showing a cross section of an original NMOS DRAM cell with one transistor and one capacitor. It was patented in 1968. The cryptanalytic machine, code-named "Aquarius", used at Bletchley Park during World War II contained a wired dynamic memory. The paper tape was read, and the characters on it “were stored in dynamic memory ... The memory used a large battery of capacitors, both charged and uncharged, the charged capacitor represented the cross (1), and the uncharged capacitor represented the dot (0 .). As the charge gradually decreased, a periodic pulse was applied to replenish the remaining charges (hence the term "dynamic"). Transistor Gate Memory Cell with Tunnel Diode Latch They replaced the gate with two transistors and two resistors, a configuration that became known as the Farber-Schlig cell. That same year they applied for a patent, but it was initially rejected. [7] In 1965, Benjamin Agusta and his team at IBM created a 16-bit silicon memory chip based on a Farber-Schlig cell with 80 transistors and 64 resistors. den and 4 diodes. The Toshiba "Toscal" BC-1411 electronic calculator, introduced in November 1965, [8][9] used a form of capacitive DRAM (180 bits) built from discrete bipolar memory cells.[8][10] The earlier forms of DRAM mentioned above used bipolar transistors. Despite better performance compared to magnetic core memory, bipolar DRAM could not compete with the lower price of magnetic core memory that was dominant at the time. Capacitors were also used in earlier memory circuits such as the Atanasoff-Berry computer cylinder, the Williams tube, and the Selectron tube. In 1966 Dr. Robert Dennard of the IBM Thomas J. Watson Research Center on MOS memory andcreate an alternative to SRAM that required six MOS transistors for each data bit. Studying the properties of MOS technology, he discovered that it could form capacitors, and storing charge or no charge on a MOS capacitor could represent the 1's and 0's bits, while the MOS transistor stored charge and could drive the capacitor. . This led to his development of a single-transistor MOS DRAM memory cell. He applied for a patent in 1967 and was granted U.S. Patent No. 3,387,286 in 1968. MOS memory offered better performance, was cheaper, and used less power than magnetic core memory. MOS DRAM chips were introduced to the market in 1969 by Advanced Memory System, Inc. from Sunnyvale, California. This 1000-bit chip was sold to Honeywell, Raytheon, Wang Laboratories and others. In the same year, Honeywell asked Intel to create DRAM using a tri-transistor cell they had developed. This became the Intel 1102 in the early 1970s. [15] However, the 1102 had many problems, prompting Intel to secretly start work on its own improved design to avoid conflicts with Honeywell. This became the first commercially available DRAM, the Intel 1103, in October 1970, despite initial low performance issues until the fifth version of the mask. The 1103 was designed by Joel Karp and constructed by Pat Earhart. The masks were cut by Barbara Maness and Judy Garcia. [16] [original research?] MOS memory overtook magnetic core memory as the dominant memory technology in the early 1970s. [14] The first DRAM with multiplexed row and column address lines was the Mostek MK4096 4-bit DRAM designed by Robert Proebsting and introduced in 1973. This addressing scheme uses the same address pins to receive the lower and upper halves of the address of the memory cell being referenced, switching between the two halves for alternating bus cycles. This was a radical advancement that effectively halved the number of address lines required, allowing it to be matched to packetspins, a price advantage that increases with each increase in memory capacity. MK4096 turned out to be a very reliable design for client applications. With a density of 16 kbit, the economic benefits increased; The 16-kilobit dynamic memory Mostek MK4116 [17] [18] introduced in 1976 took over 75% of the global DRAM memory market. However, when the density increased to 64 kbit in the early 1980s, Mostek and other American manufacturers gave way to Japanese DRAM makers who dominated the American and global markets in the 1980s and 1990s. In early 1985, Gordon Moore decided to stop producing DRAM for Intel. In 1986, all US chipmakers stopped making DRAM. In 1985, when 64K DRAM chips were the most widely used memory chips in computers, and more than 60 percent of those chips were manufactured by Japanese companies, U.S. semiconductor manufacturers accused Japanese companies of export dumping to encourage American manufacturers to trade with memory chips. Synchronous Dynamic Random Access Memory (SDRAM) was developed by Samsung. The first commercial SDRAM chip was the 16 MB Samsung KM48SL2000 [22], launched in 1992 [23]. The first commercial DDR SDRAM (Double Data Rate SDRAM) chip was the 64 MB Samsung DDR SDRAM chip released in 1998. Later in 2001, Japanese DRAM producers accused Korean DRAM producers of dumping. In 2002, US computer makers announced that they were fixing DRAM prices. Operating Principles Operating Principles for Reading a Simple Array 4 DRAM The basic structure of a DRAM array of DRAM cells is usually a rectangular array of charge storage cells, consisting of a single capacitor and a data transistor. piece. The image on the right shows a simple example with a four by four cell matrix. Some DRAM arrays consist of many thousands of cells of height and width. Long horizontal lines connecting each rowas strings of words. Each column of cells consists of two bitlines, each of which is connected to every other memory cell in the column (the image on the right omits this important information). These are commonly referred to as the "+" and "â" bitlines. A sense amplifier is basically a pair of interconnected inverters between the bit lines. The first inverter is connected to the + bit line input and the output to the bit line. The second input of the inverter is from the "bit line" with the output to the + bit line. The result is a positive feedback loop that stabilizes when one bitline reaches its highest voltage completely and the other bitline reaches its lowest possible voltage. Data bit read operations from a DRAM memory cell. Sense amplifiers are disconnected.[28] The bit lines are pre-charged to exactly the same voltage, which is between the logic high and low levels (e.g. 0.5 V when both levels are 0 and 1 V). The bit lines are physically balanced to keep the capacitance the same and therefore their voltages are equal at this point. The charging circuit is off. Since the bit lines are relatively long, they have enough capacitance to hold the pre-charged voltage for a short time. This is an example of dynamic logic.[28] The word line of the requested row is then set high to connect the cell's memory capacitor to its bit line. This causes the transistor to conduct, transferring charge from the memory location to the connected bitline (when the stored value is 1) or from the connected bitline to the memory location (when the stored value is 0). Since the bitline capacitance is usually much larger than the memory cell capacitance, the bitline voltage increases very slightly when the memory cell's capacitor discharges and decreases very slightly when the memory cell is charged (e.g. 0.45 V in both cases). Since the second bit line is 0.50V, there is a slight voltage difference between the two twisted bit lines.the sense amplifiers are now connected to pairs of bit lines. There is then positive feedback from the cross-connected inverters, thereby amplifying the small voltage difference between the odd and even row bit lines of a given column until one bit line is fully at the lowest voltage and the other at the maximum high voltage. As soon as this happens, the queue becomes "open" (data for the requested cell is available).[28] All memory cells in the open row are read simultaneously and the outputs of the read amplifier are latched. The column address then selects which latch bit to connect to the external data bus. Reading different columns in the same row can be done without delaying the opening of the row, because in the case of an open row, all data has already been exposed and bound.[28] When reading columns in an open row, current flows back along the bit line from the output of the sense amplifiers and charges the memory cells. It boosts (i.e. "restores") the charging cell by increasing the voltage across the storage capacitor if it was originally charged, or by discharging it if it was empty. Note that due to the length of the bit lines, there is a fairly long propagation delay for the transfer of charge back to the cell capacitor. This takes a significant amount of time after perceptual amplification is complete and thus coincides with the reading of one or more columns. When all columns of the current open row are read, the word line is turned off to disconnect the memory cell capacitors (the row is "closed") from the bit line. The sense amplifier is turned off and the bit lines are reloaded. Write to memory Write to DRAM cell To write data, a row is opened and the sense amplifier of that column is temporarily driven to the desired high or low voltage state, thereby causing the bit line of the cell's memory capacitor to charge or discharge to the desired value. Due to the positive feedback configuration of the sense amplifier, this will happenbit line with stable voltage even after removing the boost voltage. When writing to a particular cell, all the columns of the row are read simultaneously, just like when reading, so even if the charge on the capacitor of the memory cell changes in only one column, the entire row is updated (written back) as shown in the figure. drawing right.[28] Refresh rate Main article: Memory refresh See also: § Security Manufacturers usually specify that each line should be updated every 64 ms or less, as defined by the JEDEC standard. Some systems update each row in a batch that includes all rows every 64 ms. Other systems update one row at 64ms intervals. For example, a system with 213 = 8192 lines would require an incremental update rate of one line every 7.8 µs, which is 64 ms divided by 8192 lines. Several real-time systems update a portion of memory at a time determined by an external timer function that controls the operation of the rest of the system, such as the vertical blanking interval that occurs every 10-20 ms in a video device. The address of the next row to be updated is maintained by external logic or a counter in DRAM. The system that provides the row address (and the update command) does so to have more control over when to update and which row to update. This is done to reduce memory access conflicts, as such a system knows both memory access patterns and DRAM refresh requests. If the row address is provided by the DRAM counter, the system relinquishes control over which row is being updated and only provides an update command. Some modern DRAMs are refreshable; no external logic is required to cause the DRAM to be updated or to specify a queue address. Under certain conditions, most data in DRAM can be recovered even if the DRAM has not been updated for several minutes.[29] Times of memory Main article: MemoryMany parameters are required to fully describe DRAM runtime. Here are a few examples of two phases of DRAM asynchronous timing from a datasheet published in 1998: [30] "50 ns" "60 ns" Description tRC 84 ns 104 ns Random read or write cycle time (from one full cycle /RAS to beyond) tRAC 50 ns 60 ns Access Time: /RAS Low to Good Data tRCD 11 ns 14 ns /RAS Low to /CAS Time from Low tRAS 50 ns 60 ns /RAS Pulse Width (Minimum /RAS Low Time 30 ns) tRP 40 ns /time RAS -Precharge (min/max RAS time) tPC 20 ns 25 ns page mode read or write cycle time (/CAS to /CAS) tAA 25 ns 30 ns access time: column address valid for valid data output (including address settling time to /CAS low) tCAC 13 ns 15 ns Access time: /CAS low to valid data tCAS 8 ns 10 ns /CAS minimum pulse width This number is typically the minimum /RAS low time. It is time to open the array so that the sense enhancers will calm down. Note that the data access for one bit per line is shorter as it occurs after the read amplifier stabilizes, but the DRAM needs additional time to propagate the boosted data back to recharge the cells. The time to fetch extra bits from an open page is much shorter, determined by the cycle time from /CAS to /CAS. This number is the clearest way to compare the performance of different DRAM modules, as it places a slower limit regardless of line length or page size. Larger arrays inevitably result in larger bitline capacitance and longer propagation delays, which this time increases as the settling time of the sensitive amplifier depends on both capacitance and propagation delay. Modern DRAM chips avoid this, instead integrating many more full arrays of DRAM into a single chip to allow for more capacity without too much slowdown. When such RAM is accessed using clock logic, the time is usually rounded up to the nearest clock cycle. For example, when accessingFor example, with a 100 MHz state machine (i.e., 10 ns clock), a 50 ns DRAM can perform the first read in five clock cycles and subsequent reads on the same page every two clock cycles. This was commonly described as "5-2-2-2" time, as four readings were often done on one page. When describing synchronous memory, time is described by clock cycle counters separated by dashes. These numbers represent tCLâtRCDâtRPâTRAS as a multiple of the DRAM clock cycle time. Note that this is half the data rate when double data rate signaling is used. The PC3200's JEDEC clock frequency is 3-4-4-8[31] at 200 MHz, while the PC3200's high-performance, high-end DDR DRAM DIMMs operate at 2-2-2-5. 32 ns 5 12.5 ns 4 10 ns 9 11.25 ns 8 10 ns /CAS low to valid data output (corresponds to tCAC) tRCD 4 20 ns 2 10 ns 5 / 12.5 ns 5 / 2 ns 2 10 ns . low time tRP 4 20 ns 2 10 ns 5 12.5 ns 4 10 ns 9 11.25 ns 8 10 ns 27 33.75 ns 24 30 ns queue active time (minimum active time to initial charge) = Minimum active time to initial for charging, tRCD + tCL = 22.5 ns, and even the premium 20 ns variant is only 2.5 times better than the typical case (~2.22 times better). CAS latency improved even less, from tCAC = 13 ns to 10 ns. However, DDR3 memory achieves 32 times the bandwidth; Thanks to its internal pipeline system and wide data paths, it can output two words every 1.25ns (1600Mword/s), while the EDO DRAM can output one word per tPC=20ns (50Mword/s). Time Abbreviations tCL - CAS Latency Time tCR - Command Frequency tPTP - Precharge-to-Charge Delay tRAS - RAS Active TimeRAS-CAS Delay tREF - Refresh Period tRFC - Row Refresh Cycle Time tRP - RAS Precharge tRRD - RAS to RAS Delay tRTP - Read and Charge Delay tRTR - Read and Read Delay Write tRTW â Read - Write Delay tWR Time tWTP - Write Delay and charge tWTR - write and read delay tWTW - write and write delay) Each bit of data in DRAM is considered a positive or negative electrical charge stored in a capacitive structure. . The structure that provides the capacity and the transistors that control access to it is called a DRAM cell. They are a basic element of DRAM arrays. There are several variants of DRAM memory cells, but the most common variant in modern DRAMs is the single-transistor, single-capacitor (1T1C) cell. The transistor is used to draw current into the capacitor during write operations and to discharge the capacitor during read operations. The access transistor is designed to maximize inverter performance and minimize transistor-to-transistor leakage (Kenner, p. 34). A capacitor has two terminals, one connected to its access transistor and the other connected to ground or VCC/2. With modern DRAMs, the second case is more common, as it enables faster operation. Modern DRAM requires a +VCC/2 voltage across the capacitor to maintain logic; and -VCC/2 voltage across the capacitor is required to maintain logic zero. The electric charge stored in a capacitor is measured in coulombs. Logically, the charge is: Q = V C C 2 â C {\textstyle Q={V_{CC} \over 2}\cdot C} , where Q is the charge in coulombs and C is the capacitance in farads. The charge of logic zero is as follows: Q = â V C C 2 â C {\textstyle Q={-V_{CC} \over 2}\cdot C}.[33] A word line is required to read or write a logic zero. It is driven by a voltage greater than the sum of VCC and the threshold voltage (VTH) of the access transistor. This voltage is called VCC pumping (VCCP). TimeSo the discharge of the capacitor depends on what Boolean value is stored in the capacitor. The logic one capacitor begins to discharge when the access transistor gate voltage rises above VCCP. When the capacitor contains a logic zero, it begins to discharge when the voltage at the gate terminals exceeds VTH.[34] Capacitor Construction Up until the mid-1980s, capacitors in DRAM cells were placed in the same plane as the access transistor (they were on the surface of the substrate), hence they were called planar capacitors. The drive to increase both density and, to a lesser extent, productivity called for denser designs. This was strongly motivated by economics, which is a major factor for DRAM devices, particularly conventional DRAM. Minimizing the area of a DRAM cell can create a more dense device and reduce the cost of storing a single bit. Since the mid-1980s, the capacitor has been moved above or below the silicon substrate to achieve these goals. DRAM cells with capacitors across the substrate are referred to as layered or stacked plate capacitors. Capacitors with capacitors placed under the surface of the substrate are called trench capacitors. In the 2000s, manufacturers were sharply divided over the type of capacitor used in their DRAMs, and the relative cost and long-term scalability of the two designs was the subject of much debate. Most DRAM modules from large manufacturers such as Hynix, Micron Technology, Samsung Electronics use a multi-layer capacitor structure, while smaller manufacturers such as Nanya Technology use a trench capacitor structure (Jacob, pp. 355-357). The capacitor in a multilayer capacitor circuit is built on the surface of the substrate. The capacitor consists of an oxide-nitride-oxide (ONO) dielectric sandwiched between two layers of polysilicon wafers (the top wafer is common to all DRAM cells in the IC), and its shape can be a rectangle, cylinder, or something else to be more complex form. Here isthe basic variants of a layered capacitor based on its position relative to the bit line - the capacitor above the bit line (COB) and the capacitor below the bit line (CUB). In the former, the capacitor is below the bitline, which is usually metal, and the bitline has a polysilicon contact that extends downward to connect it to the source of the access transistor. In this second variant, the capacitor is built in via the bitline, which is almost always made of polysilicon, but is otherwise identical to the COB variant. The advantage of the COB variant is the easy contact between the bitline and the source of the access transistor, as it is physically close to the surface of the substrate. However, this requires the active area to be at a 45 degree angle when viewed from above, making it difficult to ensure that the capacitor contact does not touch the bit line. CUB cells avoid this, but have difficulty inserting contacts between bit lines because the feature size so close to the surface is equal to or close to the minimum feature size of the process technology (Kenner, pp. 33-42). A trench capacitor is constructed by etching a deep hole into a silicon substrate. Most of the substrate surrounding the hole is then heavily doped to form a buried n+ slab and reduce resistance. An oxide-nitrogen-oxide dielectric layer is grown or deposited, and finally the hole is filled by depositing doped polysilicon to form the top plate of the capacitor. The top of the capacitor is connected to the collector of the access transistor by a polysilicon bridge (Kenner, pp. 42–44). The channel capacitor depth-to-width ratio of mid-2000s DRAMs can exceed 50:1 (Jacob, p. 357). Channel capacitors have many advantages. Since the capacitor is buried in most of the substrate rather than on its surface, the area it occupies can be minimized to that required to connect it to the access transistor.outlet without reducing the size of the capacitor and thus the capacity (Jacobs, pp. 356-357). Alternatively, the capacitance can be increased by etching a deeper hole without increasing the surface area (Kenner, p. 44). Another advantage of trench capacitors is that their structure is below the metal interconnect layers, which facilitates their alignment, allowing integration into a logic-optimized workflow that has many interconnect levels above the substrate. . The fact that the capacitor is below logic means it was designed before transistors. This allows capacitors to be manufactured in high-temperature processes that would otherwise degrade logic transistors and their performance. This makes trench capacitors suitable for creating embedded DRAM (eDRAM) memory (Jacob, p. 357). The disadvantages of trench capacitors are the difficulty of reliably manufacturing the capacitor structures in deep wells and connecting the capacitor to the collector terminal of the output transistor (Kenner, p. 44). Historical cell design The first generation of DRAM ICs (1Kb capacity), the first of which was the Intel 1103, used a three-transistor, one-capacitor (3T1C) DRAM cell. In the second generation, the requirement to increase density by placing more bits in a given area, or the requirement to reduce cost by placing the same number of bits in a smaller area, led to the near-universal adoption of the 1T1C DRAM cell. although some 4K and 16K devices continued to use the 3T1C cell for performance reasons (Kenner, p. 6). Among these performance advantages was the ability to read the stored state of the capacitor without discharging it, without the need to overwrite the reading (non-destructive reading). A second performance advantage is that the 3T1C cell has separate read and write transistors; the memory controller can use this functionperform an atomic read-modify-write where a value is read, modified, and then written back as one indivisible operation (James, p. 459). Suggested Cell Models The single-transistor, capacitorless (1 T) DRAM cell has been the subject of research since the late 1990s. 1T DRAM is a different way of building a basic DRAM memory cell than the classic single transistor/single capacitor (1T/1C) DRAM cell, sometimes referred to as "1T DRAM", especially when compared to 3T and 4T. It replaced DRAM in the 1970s. In 1T DRAM cells, data bits are still stored in a capacitive region controlled by a transistor, but this capacitance is no longer provided by a separate capacitor. 1T DRAM is a "capacitorless" bit cell design that stores data using the parasitic body capacitance inherent in silicon-on-insulator (SOI) transistors. This floating body effect is considered a logical design difficulty and can be used to store data. This provides the highest density of 1TB DRAM cells and also makes it easier to integrate high performance logic circuits as they are built using the same SOI technologies. Cell refresh is still required, but unlike 1T1C DRAM, reading 1T DRAM will not destroy them; the accumulated charge causes a noticeable shift in the threshold voltage of the transistor.[35] In terms of performance, access times are significantly better than capacitor DRAM, but slightly worse than SRAM. There are several types of 1T DRAM: commercial Z-RAM from Innovative Silicon, TTRAM[36] from Renesas, and A-RAM from the UGR/CNRS consortium. Array Structures Self-aligning storage node placement simplifies the manufacturing process of today's DRAMs.[37] DRAM cells are arranged in a conventional rectangular grid to make them easier to manage and access using words and bit strings. The physical arrangement of DRAM cells in an array is usually designed such that two adjacent DRAM cells in a column share one.contacts reduce their area. The area of a DRAM cell is specified as n F2, where n is a number derived from the DRAM cell design and F is the smallest cell size of a particular process technology. This scheme allows comparison of DRAM size across process generations because the DRAM cell area varies linearly or nearly linearly with cell size. A typical area of modern DRAM cells ranges from 6 to 8 F2. A horizontal wire, the word line, is connected to the gate of each access transistor in its row. The vertical bit line is connected to the transistor source in its own column. Words and bit strings have a limited length. The length of the word chain is limited by the required array power, since the signal propagation time that must travel through the word bus is determined by the RC time constant. The length of a bit line is limited by its capacity (which increases with length), which must be in range to be read correctly (since DRAM works by detecting the charge on a capacitor released on the bit line). The length of the bit line is also limited by the amount of operating current that the DRAM can draw and how the power can be dissipated, these two characteristics being largely determined by the charging and discharging of the bit line. Bit line architecture Sense amplifiers are required to read the state in the DRAM cells. When the access transistor is activated, the electric charge in the capacitor is shared by the bit line. The capacity of the bit line is much larger than the capacity of the capacitor (about ten times). The voltage changes on the bit line are therefore negligible. Sense amplifiers are required to convert the voltage difference to levels determined by the logic signaling system. Modern DRAMs use differential sense amplifiers and have DRAM array design requirements. Differential sense amplifiers work by biasing their output signals to opposite limits based onvoltage on pairs of bit lines. Sense amplifiers only work effectively and efficiently when the capacitance and voltage of these bitline pairs are closely matched. In addition to ensuring that the lengths of the bitlines and the number of DRAM cells connected to them are the same, the array design has resulted in two basic architectures that meet the requirements of sense amplifiers: open and stacked bit arrays. Open bit fields First generation (1 Kbit) DRAM ICs up to the 64 Kbit generation (and some 256 Kbit devices) had an open bit line field architecture. In these architectures, the bitlines are divided into multiple segments and differential amplifiers are placed between the bitline segments. Since sense amplifiers are placed between bitline segments to route their output from the array, an additional layer of connections is required over and above those used to create wordlines and bitlines. DRAM cells located at the edges of the array have no adjacent segments. Since differential amplifiers require the same capacitance and bitline length for both segments, dummy bit segments are available. An open bit field has the advantage of having a smaller field area, although this advantage is somewhat offset by dummy bit segments. The disadvantage that led to the near demise of this architecture is its inherent susceptibility to noise, which affects the performance of differential amplifiers. Since each bitline segment has no spatial relation to the other, it is possible for noise to affect only one of the two bitline segments. Convoluted Bitline Arrays The convoluted bitline array architecture routes bitlines in pairs through an array. The close proximity of paired bitlines provides better common-mode noise suppression characteristics compared to open bitfields. Stacked architecture of bitline tables started to emerge during DRAM ICfrom the 256 Kbit generation. This architecture is popular in modern DRAM ICs due to its excellent noise immunity. This architecture is called foldable because it is based on an open array architecture from a circuit diagram perspective. The complex matrix architecture appears to remove DRAM cells from a column in alternating pairs (since two DRAM cells share a common bit contact) and then move DRAM cells from an adjacent column into empty slots. The place where the bit line rotates takes up extra space. To minimize overhead areas, engineers choose the simplest and minimal spin scheme that can reduce noise below a certain threshold. As process technology improves to reduce the minimum component size, the signal-to-noise problem worsens because the coupling of adjacent metal wires is inversely proportional to their pitch. The field convolution and bitwise convolution schemes used must increase in complexity to maintain sufficient noise reduction. Schemes that have desirable noise immunity properties with minimal area impact are the subject of ongoing research (Kenner, p. 37). Future field architectures Advances in process technology may favor open bitline field architectures if they can provide better long-term field performance; as complex array architectures require increasingly complex assembly schemes to accommodate any advancement in process technology. The relationship between process technology, array architecture, and area performance is an active area of research. Row and Column Redundancy The first DRAM chips had no redundancy. An IC with a defective DRAM cell will be rejected. Starting with the 64K

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